WORLD TRADE ORGANIZATION

IP/N/1/EST/7
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24 August 2023

(23-5701)

Council for Trade-Related Aspects of Intellectual Property Rights

Original: English

NOTIFICATION OF LAWS AND REGULATIONS UNDER ARTICLE 63.2 OF THE TRIPS AGREEMENT

ESTONIA: LAYOUT-DESIGNS OF INTEGRATED CIRCUITS PROTECTION ACT

Notifying Member	**ESTONIA**

Details of the notified legal text

Title	Layout-Designs of Integrated Circuits Protection Act
Subject matter	Layout-designs (topographies) of integrated circuits
Nature of notification	[X] Main dedicated intellectual property law or regulation [ ] Other law or regulation
Link to legal text*	https://ip-documents.info/2023/IP/EST/23_11798_00_e.pdf
Notification status	[ ] First notification [X] Amendment or revision to notified legal text [ ] Replacement or consolidation of notified legal text(s)
Previous notification(s) referred to	IP/N/1/EST/L/1
Brief description of the notified legal text This Act regulates the legal protection of layout-designs of integrated circuits.	
Language(s) of notified legal text	English
Entry into force	1 April 2019; Initial date of entry into force 16.03.1998 Latest amendments 01.04.2019
Other date	

Notification details

Submission date of notification	14 June 2023
Other information	

Agency or authority responsible	Estonian Ministry of Justice Email: info@just.ee Website: https://www.just.ee/en

* Links are provided to texts of laws and regulations notified under the TRIPS Agreement in the form supplied by the Member concerned; the WTO Secretariat does not endorse or revise their content.